This Page Is Inserted by IFW Operations
and is not a part of the Official Record

BEST AVAILABLE IMAGES

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

IMAGES ARE BEST AVAILABLE COPY.

As rescanning documents *will not* correct images, please do not report the images to the Image Problem Mailbox.

OIPE JC151
JUN 14 2004
PATENT & TRADEMARK OFFICE

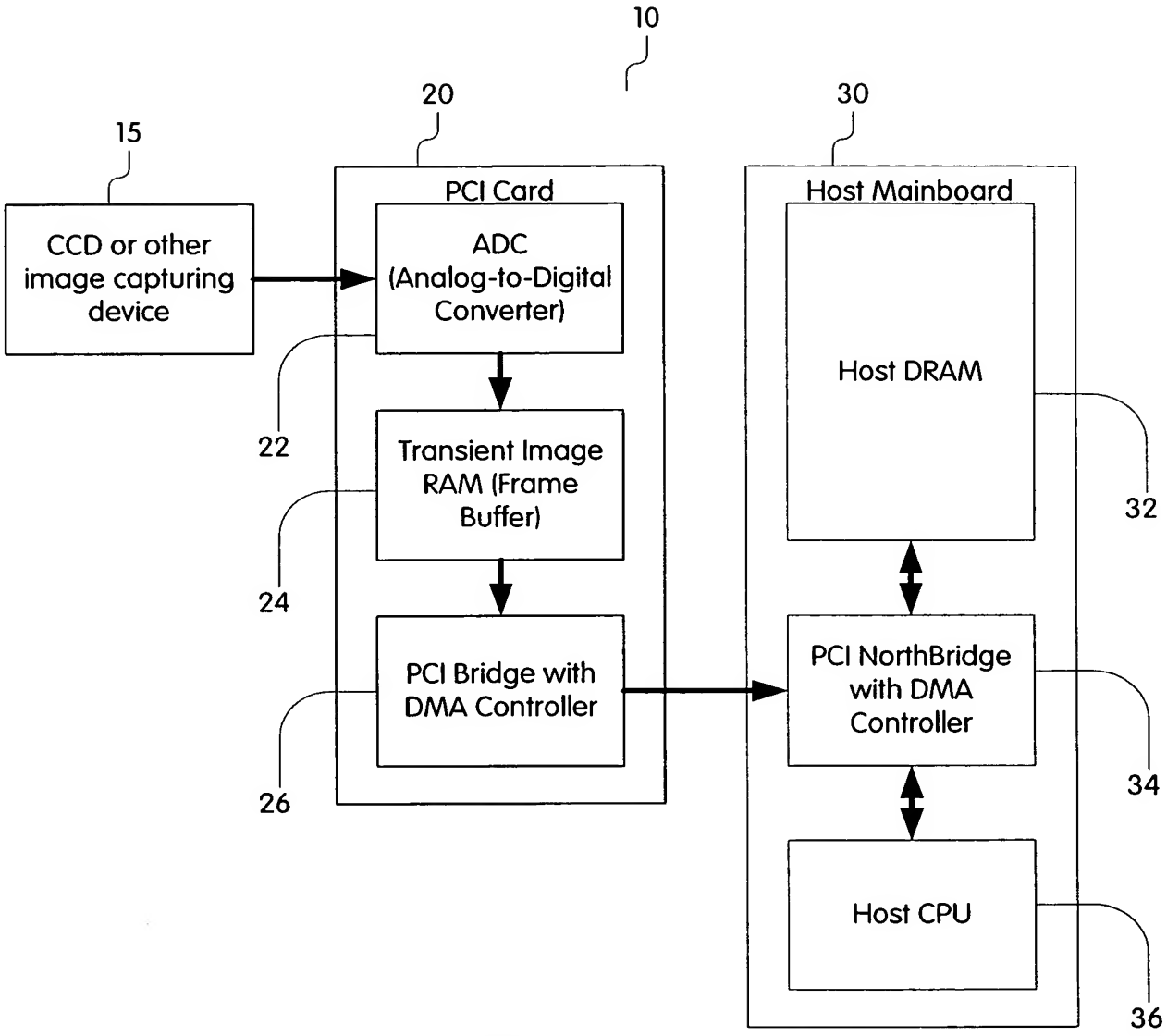

Fig. 1
(Prior Art)

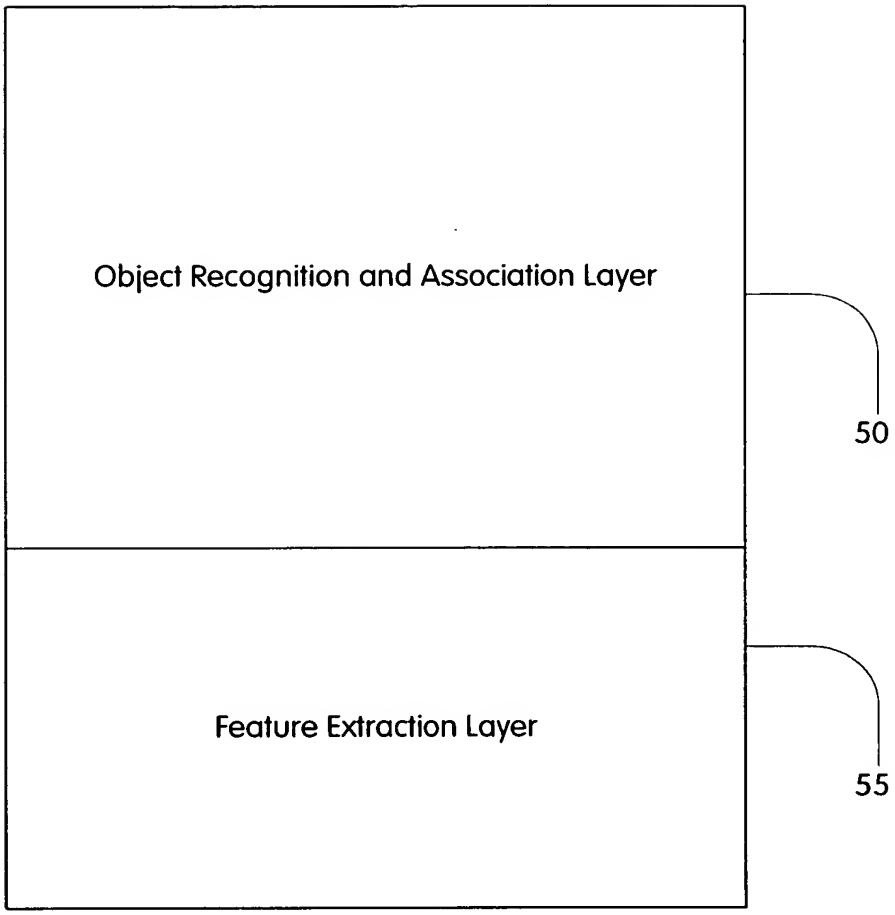

Fig. 2
(Prior Art)

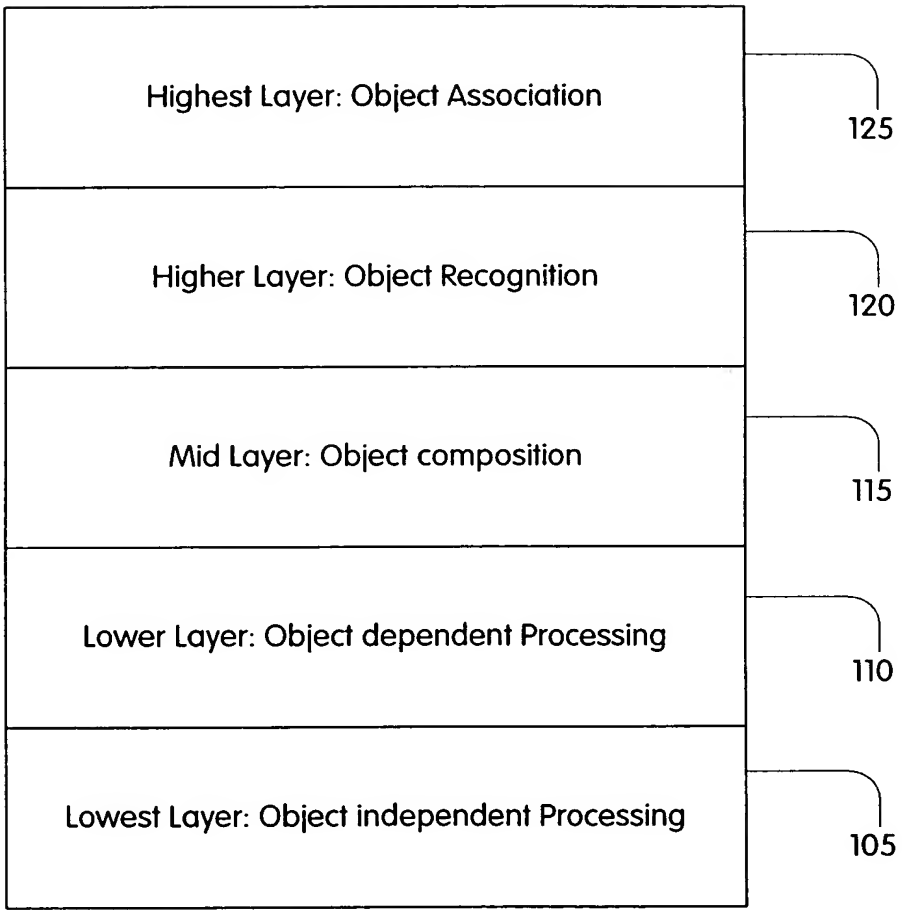
Highest Layer: Object Association
125
Higher Layer: Object Recognition
120
Mid Layer: Object composition
115
Lower Layer: Object dependent Processing
110
Lowest Layer: Object independent Processing
105

Fig. 3

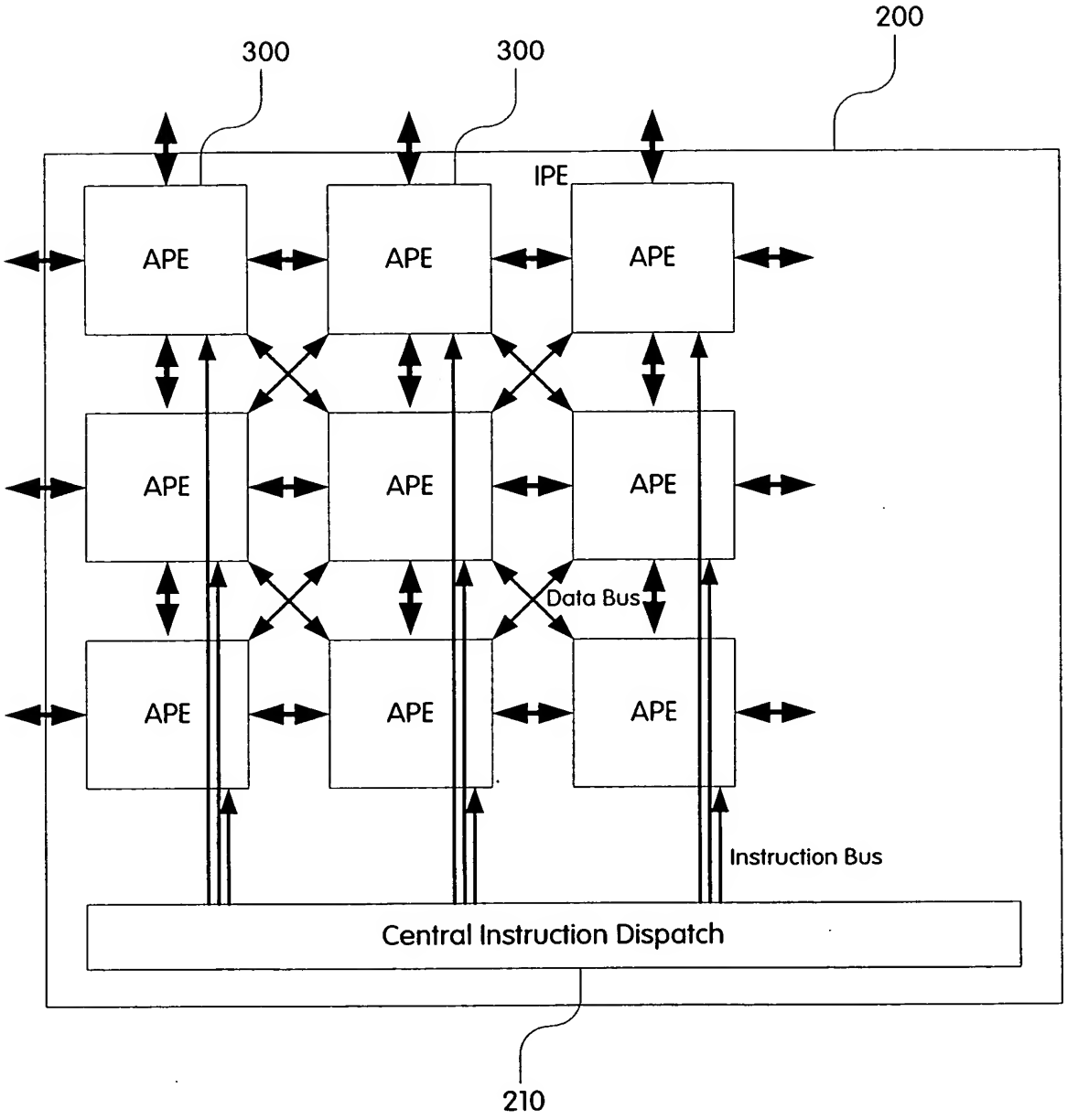
200
300
300
IPE
APE
APE
APE
APE
APE
APE
APE
APE
APE
Data Bus
Instruction Bus
Central Instruction Dispatch
210

Fig. 4

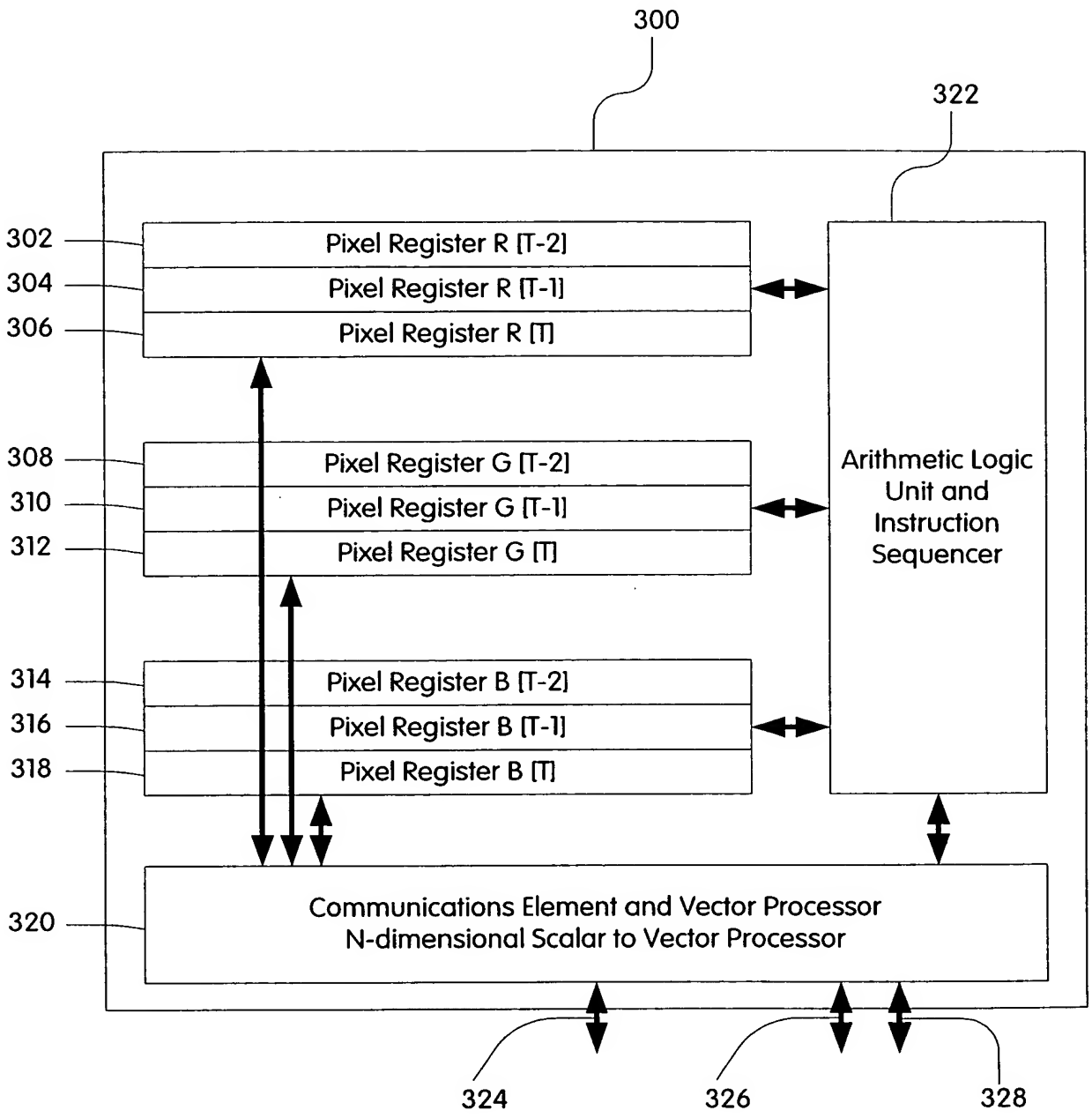
300
322
302
304
306
Pixel Register R [T-2]
Pixel Register R [T-1]
Pixel Register R [T]
308
310
312
Pixel Register G [T-2]
Pixel Register G [T-1]
Pixel Register G [T]
314
316
318
Pixel Register B [T-2]
Pixel Register B [T-1]
Pixel Register B [T]
Arithmetic Logic Unit and Instruction Sequencer
320
Communications Element and Vector Processor
N-dimensional Scalar to Vector Processor
324
326
328

Fig. 5

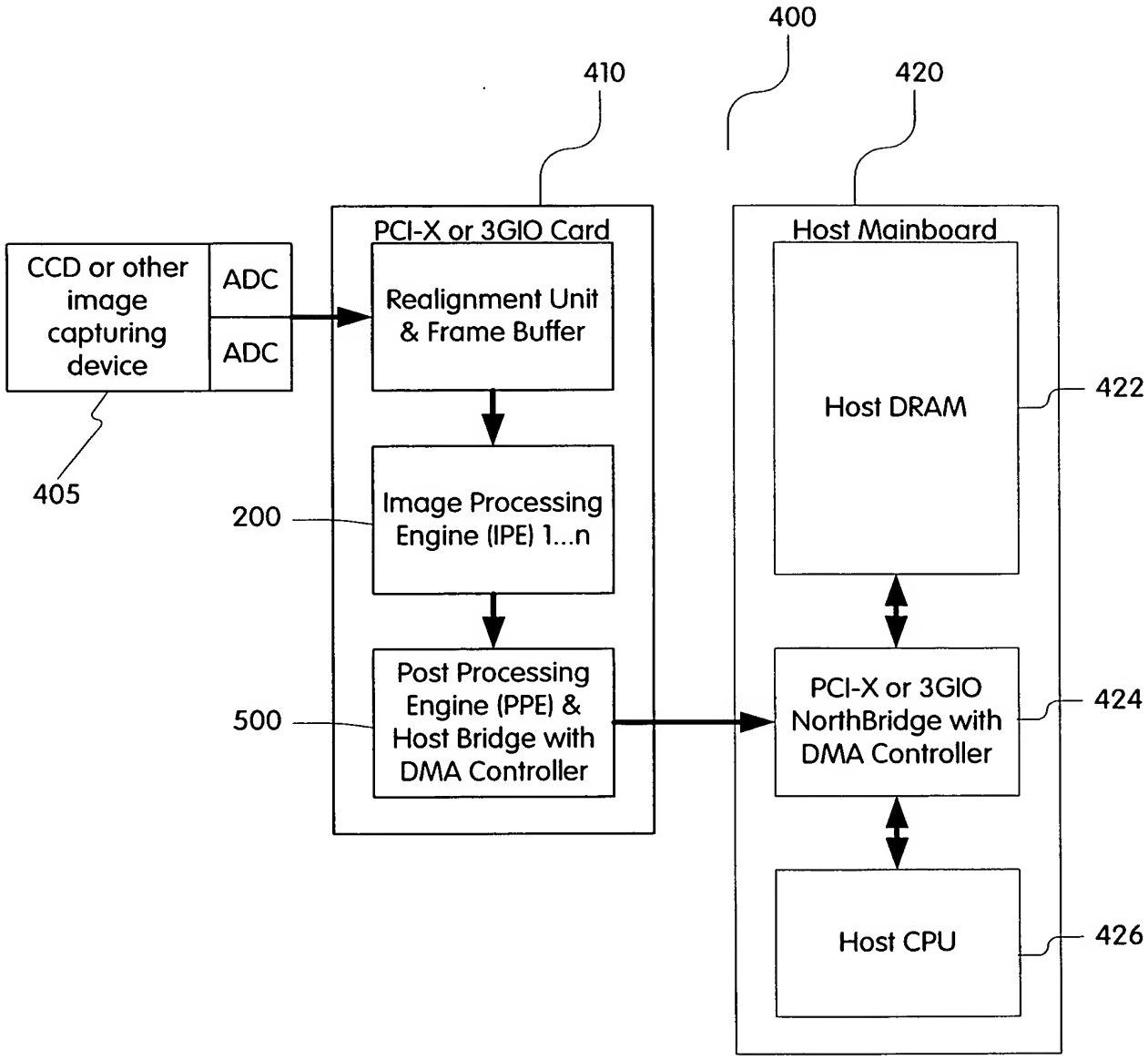
400
410
420
PCI-X or 3GIO Card
Host Mainboard
CCD or other image capturing device
ADC
ADC
Realignment Unit & Frame Buffer
Host DRAM
422
405
200
Image Processing Engine (IPE) 1...n
500
Post Processing Engine (PPE) & Host Bridge with DMA Controller
PCI-X or 3GIO NorthBridge with DMA Controller
424
Host CPU
426

Fig. 6